Data compression

Data compression will reduce all particle count data to 8 bit words. The compression will meet two requirement - it will be linear for small numbers and will give approximately square-root compression for large numbers. The top end will become logarithmic when the resolution reaches about 2%. The capacity of the counters is 14 bits, and will typically not have rates that fill the counter. The averaging circuit will have 16 bit capacity. Three compression modes are considered, for 14, 15, and 16 bits. A single circuit can be programmed to give the desired compression. The planned approach is to use a method similar to the quasi-log compression used on the rockets. The position of the most signifcant non-zero bit is located and encoded for the high bits of the output word. The bits following the first "1" are appended as the low order bits of the output word.

The following tables define the compression. The column #Steps is the total number of steps in the linear chord that makes of each octave. The corresponding step size is the number of counts represented by one step. The step size can be compared with the variance (sq-root) of the counts.

	14 Bits range		15 Bits range		16 bits range		
Counts	#Steps	Size	#Steps	Size	#Steps	Size	Sq-root
0 - 15	16	linear	16	linear	16	linear	
16 - 31	8	2	8	2	8	2	5.6
32 -	8	4	8	4	8	4	8
64 -	16	4	16	4	16	4	11.3
128 -	16	8	16	8	16	8	16
256 -	16	16	16	16	16	16	23
512 -	16	32	16	32	16	32	32
1024 -	32	32	32	32	16	64	45
2048 -	32	64	32	64	16	128	64
4096 -	32	128	32	128	32	128	91
8K -	64	128	32	256	32	256	128
16K -			32	512	32	512	181
32K -					32	1024	256

Bit patterns for MSBs

	14 Bit	15 Bit	16 Bit
16			111xxxxx
15		111xxxxx	110xxxxx
14	11xxxxxx	110xxxxx	101xxxxx
13	101xxxxx	101xxxxx	100xxxxx
12	100xxxxx	100xxxxx	0111xxxx
11	011xxxxx	011xxxxx	0110xxxx
10	0101xxxx	all same from here down	
9	0100xxxx		
8	0011xxxx		
7	0010xxxx		
6	00011xxx		
5	00010xxx		
4	00001xxx (linear from here down)		
3	00000xxx		
2	00000xxx		
1	00000xxx		

The rocket style compressor uses a state machine to define the sequence of operations that depends on the contents of the incoming data. The FAST compression will use a variable length "characteristic", so 2 additional bits are used to indicate the number bit shifts required for the "mantissa" position. The state machine counts the number of data shifts before the first "1" appears. The output of the state machine will determine the data that will be loaded into the "characteristic" and the shift position of the following "xxxx" mantissa bits that are attached.

Codes for state machine: The leading two bits indicate the number of "x" bits used; 11 = 6 bits, 10 = 5, 01 = 4, and 00 = 3 bits. The leading bits are also cyclical so only 5 bits are needed for the state machine. The gaps in the table are implicitly "0".

	14 Bit	15 Bit	16 Bit
16			10111xxxxx
15		10111xxxxx	10110xxxxx
14	1111xxxxxx	10110xxxxx	10101xxxxx
13	10101xxxxx	10101xxxxx	10100xxxxx
12	10100xxxxx	10100xxxxx	01 111xxxx
11	10011xxxxx	10011xxxxx	01 110xxxx
10	01 101xxxx	all same from here down	
9	01 100xxxx		
8	01 011xxxx		
7	01 010xxxx		
6	00 011xxx		
5	00 010xxx		
4	00 001xxx (linear from here down)		
3	00 000xxx		
2	00 000xxx		
1	00 000xxx		

The following operations will generate the desired states:

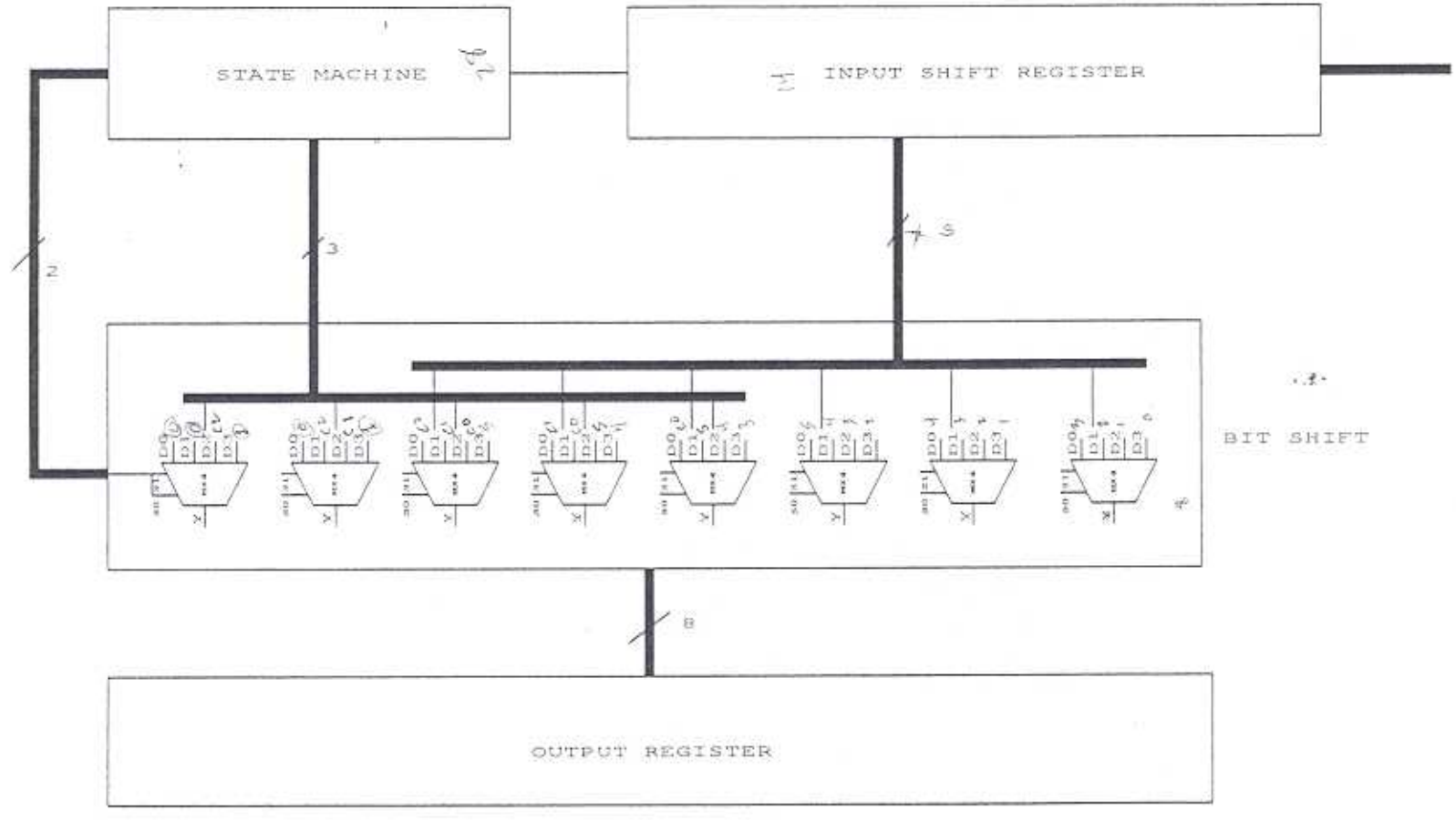
Preset values for first cycle: if M14, set 11110, else 10111

The first 2 MSBs decrement from the following states:

A 1111x	
B 10011	(set next state xx101)
C 01010 and not M16	(set next state xx011)
D 10100 and M16	(set next state xx111)

The remaining bits decrement as normal binary counters except for the branch states B, C, and D. The new states can generated by the following operations.

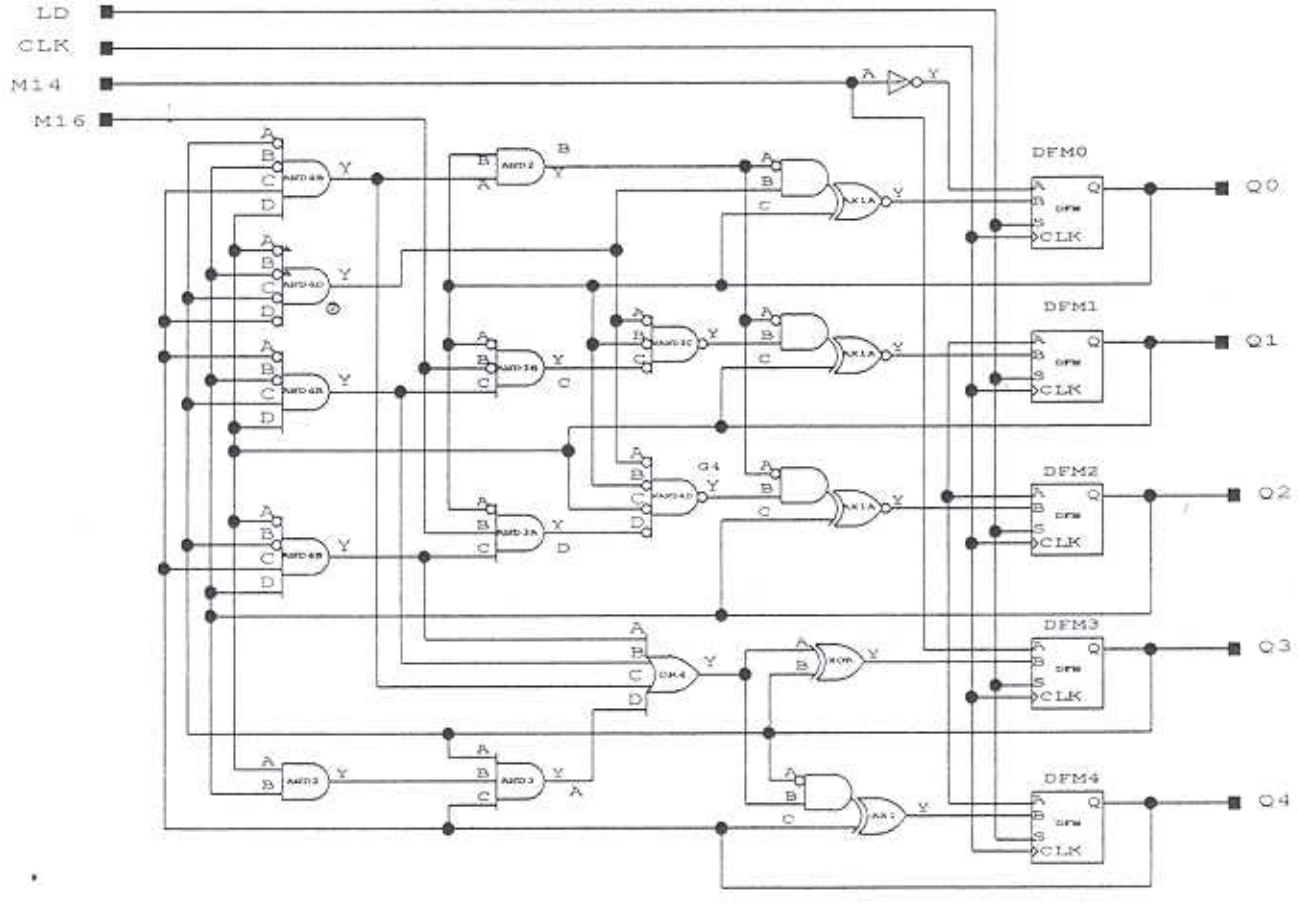
B Set 101 from 011	Enable toggle on Q1 and Q2, inhibit Q0.
C Set 011 from 010	Inhibit Q1
D Set 111 from 100	Inhibit Q2



FAST/SMEX
SPACE SCIENCES LABORATORY
UNIVERSITY OF CALIFORNIA, BERKELEY

TITLE: DATA COMPRESSOR

DATE: 8/10/92 | DRAWN BY: C W CARLSON



28 MODULES

FAST/SMEX
SPACE SCIENCES LABORATORY
UNIVERSITY OF CALIFORNIA, BERKELEY

TITLE: COMPRESSOR STATE MACHINE

DATE: 8/10/92 | DRAWN BY: C W CARLSON

FAST COMPRESSION MAPS
7 April 1993 D.W.Curtis

Input Word is:

MSB															LSB
DF	DE	DD	DC	DB	DA	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

MSL is the number of the most significant non-zero bit (0-15)

14->8 (ESA Burst, WPC, TEAMS)

Input	Output Byte								
MSL	7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	D0	
1	0	0	0	0	0	0	D1	D0	
2	0	0	0	0	0	D2	D1	D0	
3	0	0	0	0	1	D2	D1	D0	
4	0	0	0	1	0	D3	D2	D1	
5	0	0	0	1	1	D4	D3	D2	
6	0	0	1	0	D5	D4	D3	D2	
7	0	0	1	1	D6	D5	D4	D3	
8	0	1	0	0	D7	D6	D5	D4	
9	0	1	0	1	D8	D7	D6	D5	
10	0	1	1	D9	D8	D7	D6	D5	
11	1	0	0	DA	D9	D8	D7	D6	
12	1	0	1	DB	DA	D9	D8	D7	
13	1	1	DC	DB	DA	D9	D8	D7	
14	1	0	1	DD	DB	DA	D9	D8	<*>
15	1	0	0	DE	DD	DB	DA	D9	<*>

16->8 (ESA Avg., TEAMS)

Output Byte							
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	D0
0	0	0	0	0	0	D1	D0
0	0	0	0	0	D2	D1	D0
0	0	0	0	1	D2	D1	D0
0	0	0	1	0	D3	D2	D1
0	0	0	1	1	D4	D3	D2
0	0	1	0	D5	D4	D3	D2
0	0	1	1	D6	D5	D4	D3
0	1	0	0	D7	D6	D5	D4
0	1	0	1	D8	D7	D6	D5
0	1	1	0	D9	D8	D7	D6
0	1	1	1	DA	D9	D8	D7
1	0	0	DB	DA	D9	D8	D7
1	0	1	DC	DB	DA	D9	D8
1	1	0	DD	DC	DB	DA	D9
1	1	1	DE	DD	DC	DB	DA

<*> Illegal Input

12->8 BBF

Input	Output Byte							
MSL	7	6	5	4	3	2	1	0
3	0	0	0	0	0	0	0	D3
4	0	0	0	0	0	0	D4	D3
5	0	0	0	0	0	D5	D4	D3
6	0	0	0	0	D6	D5	D4	D3
7	0	0	0	D7	D6	D5	D4	D3
8	0	0	1	D7	D6	D5	D4	D3
9	0	1	0	D8	D7	D6	D5	D4
10	0	1	1	D9	D8	D7	D6	D5
11	1	0	0	DA	D9	D8	D7	D6
12	1	0	1	DB	DA	D9	D8	D7
13	1	1	0	DC	DB	DA	D9	D8
14	1	1	1	DD	DC	DB	DA	D9